Improving Physical Verification Performance and Productivity for Latest GPU Designs

Synopsys / NVIDIA

ABSTRACT

Nvidia designs some of the largest and most complex chips in the world. With increasing DRC complexity at advanced technology nodes and large design sizes, physical verification turnaround time is a key challenge to deliver tape-outs on schedule.

This paper discusses Nvidia's physical verification methodology with IC Validator and how this methodology was successfully deployed on latest designs to achieve fast performance and improved productivity.

SYNOPSYS
Silicon to Software

Improving Physical Verification Performance and Productivity for Latest GPU Designs

NVIDIA Experience

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Manoz Palaparthi, Technical Marketing Manager, Synopsys

September 13, 2017

Today's Presentation

IC Validator Technology Overview

Manoz Palaparthi
Synopsys

NVIDIA Experience with IC Validator for Latest GPU Designs

Ramulu Undevalli
NVIDIA

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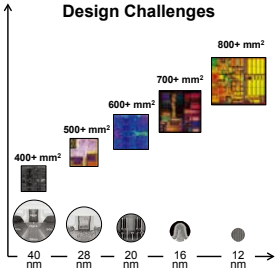
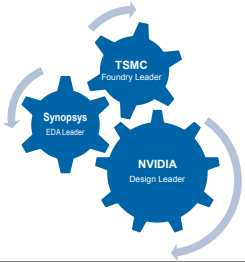
Strong Collaboration with TSMC and Leading Customers

Advanced Node Design Challenges



Ecosystem Collaboration to Drive Success



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IC Validator Comprehensive Physical Verification Solution

DRC	•Polygon spacing and width rules •Complex rules (>5,000) for advanced processes
Pattern Matching	•Auto-fixing with In-design •Mixed DRC rules that include patterns
Multi-Patterning	•Double patterning •Triple patterning •Verification, decomposition, coloring, and fixing
LVS	•Device extraction •Compare reference to extracted netlists •Device parameter extraction •Integration with StarRC
Electrical Rule Checking	•Basic checks •Shorts/opens
Extended ERC	•Multi-voltage region rules •Electrostatic discharge checks •Current-density checks •Point-to-point resistance checks

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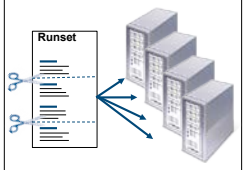
IC Validator Performance and Scalability

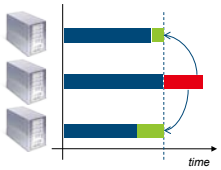
Massively parallel distributed processing technology

Linear Scalability



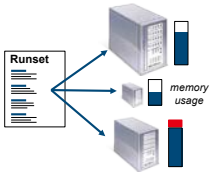
Parallelize tasks across machines and cores

Smart Load Sharing



Send jobs to cores that are not busy

Memory Aware Scheduling



Avoid exceeding memory limits

5.6X better performance from 16 to 96 CPUs

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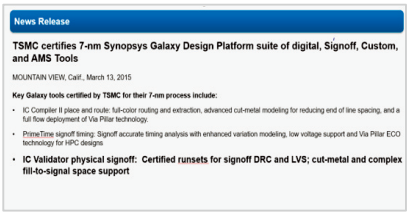
Foundry Certified for Advanced Processes

IC Validator

Node	tsmc		
	DRC	LVS	FILL
65	✓	✓	✓
40	✓	✓	✓
28	✓	✓	✓
20	✓	✓	✓
16	✓	✓	✓
10	✓	✓	✓
12	✓	✓	✓
7	✓	✓	✓



News Release

TSMC certifies 7-nm Synopsys Galaxy Design Platform suite of digital, Signoff, Custom, and AMS Tools

MOUNTAIN VIEW, Calif., March 13, 2015

Key Galaxy tools certified by TSMC for their 7-nm process include:

- IC Compiler II place and route: full-color routing and extraction, advanced cut-metal modeling for reducing end of line spacing, and a full flow deployment of Via Pillar technology.
- PrimeTime signoff timing: Signoff accurate timing analysis with enhanced variation modeling, low voltage support and Via Pillar ECO technology for HPC designs
- **IC Validator physical signoff: Certified runsets for signoff DRC and LVS; cut-metal and complex fill-to-signal space support**

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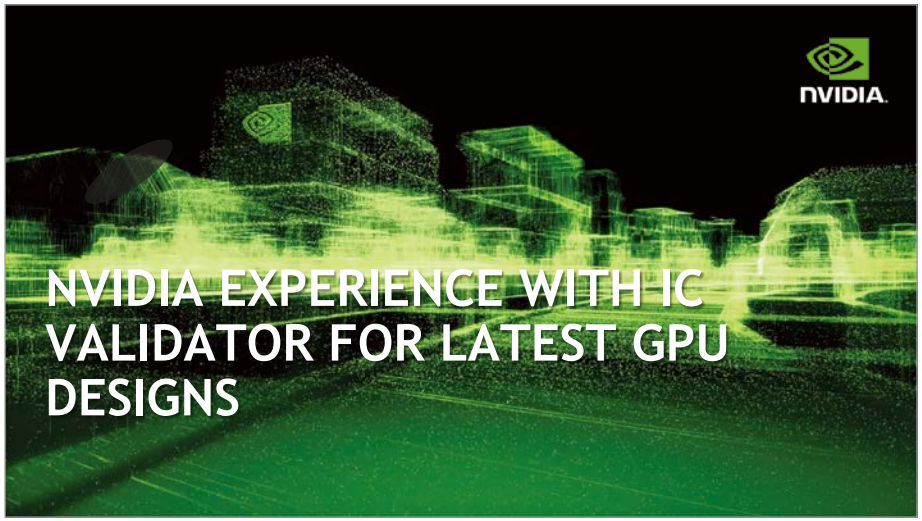

NVIDIA - THE AI COMPUTING COMPANY

World Leader in AI Computing

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SCHEDULE CHALLENGES AT NEW NODES

- Technology nodes progressing much faster, increasing time pressure to production flows
- Close collaboration with TSMC and Synopsys
  - Engage with TSMC on runset enablement early in the process development cycle
  - Engage with Synopsys on early runset validation for new silicon technology nodes

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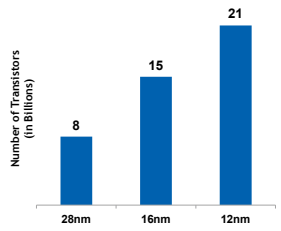
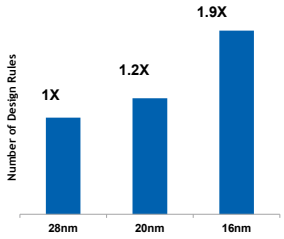
PHYSICAL VERIFICATION CHALLENGES AT ADVANCED NODES

Big and Complex Designs



Increasing DRC Rules and Complexity



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THE LARGEST GPUS WITH THE HIGHEST PERFORMANCE

- NVIDIA's largest production GPU
  - 815 mm^2
  - 21 Billion transistors
  - 148 unique partitions (tiles/blocks)
- TSMC 12 nm with 14 metal layers

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NVIDIA'S PHYSICAL VERIFICATION REQUIREMENTS

Performance & Productivity

- Overall Turn-around Time
  - Block level as well as Full chip
  - DRC, LVS, Antenna Runtime Performance
  - Debugging errors

Design	Target Runtime
Small P&R block	2 to 3 hrs
Large P&R block	10 hrs
Full chip	1 to 1.5 days

Advanced Technology

- Runsets for new technology
  - Early access to runsets
  - Customized rules

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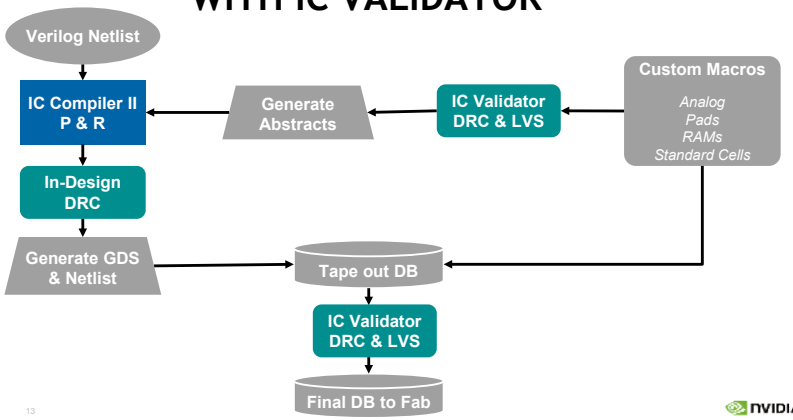
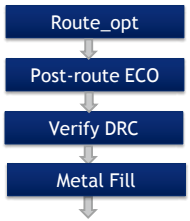
NVIDIA'S FULL CHIP DESIGN FLOW WITH IC VALIDATOR



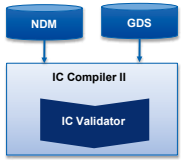
BLOCK VERIFICATION: IN-DESIGN IN IC COMPILER II

Block Verification Flow



In-Design IC Validator

- GDS merge flow for signoff accurate verification and debugging
  - Verify full design including internal cell layout



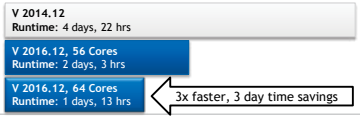
FULL CHIP SIGNOFF DRC RESULTS

Run Configuration

- IC Validator 2016.12 version
- Distributed processing
  - 8x 1TB machines
  - 8 cores per machine

Performance Results

- Runtime: 1 day, 13 hrs
- Peak memory: 436 GB
- IC Validator
  - Over 40% lower memory
  - Command specific speed up
  - Improved CPU scalability



DISTRIBUTING DRC JOB ACROSS MACHINES

Analysis of the physical verification job efficiency

- IC Validator deploys both distributed processing and multi-threading based on available cores
- Close to 100% CPU utilization across cores
- Scheduler efficiently scheduled jobs to stay within available resources

NEXT STEPS

- Collaborate with Synopsys to meet targets for next generation GPU projects
  - Identify performance critical areas (e.g. chip assembly) in NVIDIA verification flow
  - Enhance full chip signoff runtime performance

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SUMMARY

- NVIDIA is tackling the largest and most challenging designs in the industry today
- IC Validator is our primary physical verification tool for DRC and LVS
- IC Validator's multi-CPU scalability has enabled NVIDIA to verify some of the largest and most complex designs in the industry

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THANK YOU